Abstract of the Disclosure

A method and apparatus to correctly compute a vector-gather, vector-operate (e.g., vector add), and vector-scatter sequence, particularly when elements of the vector may be redundantly presented, as with indirectly addressed vector operations. For an add operation, one vector register is loaded with the "add-in" values, and another vector register is loaded with address values of "add to" elements to be gathered from memory into a third vector register. If the vector of address values has a plurality of elements that point to the same memory address, the algorithm should add all the "add in" values from elements corresponding to the elements having the duplicated addresses. An indirectly addressed load performs the "gather" operation to load the "add to" values. A vector add operation then adds corresponding elements from the "add in" vector to the "add to" vector. An indirectly addressed store then performs the "scatter" operation to store the results.

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